Call For Papers

10th IEEE Electron Devices Technology and Manufacturing (EDTM 2026) Conference

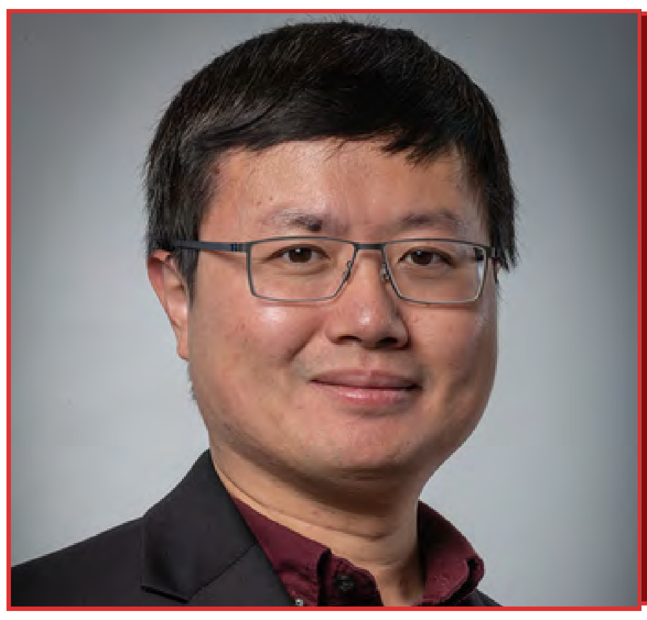
100 YEARS
FIELD-EFFECT TRANSISTOR
1-4 MARCH, 2026

edtm 2026
Electron Devices Technology and Manufacturing Conference

EDTM 2026 Plenary / Keynote Speakers

Prof. Subramanian S. Iyer

UCLA Center for Heterogeneous Integration and Performance Scaling
Samueli School of Engineering
University of California



Prof. Hiu Yung Wong

Vice Chair, Academic Senate
Electrical Engineering,
San Jose State University

Mr Dakshina Murthy

Srikanteswara Fellow,
Foundry
Technology Operations,
Advanced Micro Devices,
Singapore

Dr Digh Hisamoto

Senior chief researcher,
Hitachi, Ltd., Tokyo, Japan.
2019 Andrew S Grove Award
IEEE Fellow

Prof. Hiroshi Iwai

Tokyo Institute of Technology, Yokohama,
Japan

Dr Manish Chhowalla

Goldsmiths' Professor of Materials Science at the University of Cambridge.

Dr Angelo Pinto

IEEE Fellow
Vice President
Intel Corp

- **Accepted and presented papers will be submitted for inclusion into IEEE Xplore subject to meeting IEEE Xplore's scope and quality requirements.**
- **The authors of a selected number of high-impact papers will be invited to submit extended versions for publication in the special issue of IEEE Journal of Electron Devices Society (J-EDS) and IEEE Transactions on Materials for Electron Devices (T-MAT), subjected to J-EDS and T-MAT policies.**

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Electron Devices Society

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EDTM 2026 FOCUS SESSION

Focus Session 01:

Quantum Neural Network, QNN

Chair:
Han Wang

The University of Hong Kong

Focus Session 02:

Bio-hybrid electronics

Chair:
Anna Maria Pappa

Khalifa University, United Arab Emirates (UAE)

Focus Session 03:

On-Chip Thermal Management

Chair:
Sayani Majumdar

Tampere University, Finland

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Plenary Speaker

Prof. Subramanian S. Iyer

UCLA Center for Heterogeneous Integration and Performance Scaling

Subramanian S. Iyer (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is the founding Director of the Center for Heterogeneous Integration and Performance Scaling (UCLA CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. Since joining UCLA, he has been exploring new packaging paradigms and device innovations that may enable wafer-scale architectures, in- memory analog compute and medical engineering applications. He is a fellow of IEEE, APS, iMAPS and NAI as well as a Distinguished Lecturer of IEEE EDS and EPS. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012 and the 2020 iMAPS Daniel C. Hughes Jr Memorial award and the iMAPS distinguished educator award in 2021. Prof. Iyer was also Prof. Ramakrishna Rao Visiting Chair Professor at IISc, Bengaluru.

Strategic Directions for Electronics Packaging

Recent advances in electronics packaging have come to the rescue as CMOS scaling has stalled making possible the incredible advances in AI/ML and many other fields, that promise to transform our lives. This journey, however, has only just begun and much more is yet to come. The key features that will drive this transformation can be described with the simple strategy of "scale-down and scale-out" that has characterized monolithic CMOS scaling for several decades, the drive to chiplets with higher yields, and the ability to assemble a diversity of technologies on the same substrate allowing us to blur the lines between monolithic chip and a large heterogeneous assembly of chips. In this talk we will describe our approach to simplify packaging at all levels: from design, architecture, process and manufacturing that have the potential to take packaging to the next level including the ability to scale packaging systematically. If time permits, we will outline how to meet those challenges through a broad and organic Industry-Academia Coalition called ÆPeX America – the Advanced Electronics Packaging eXchange for America. We will outline how companies (small and large), research establishments and Universities can join ÆPeX America and benefit and contribute to our progress.

Conference Tracks

- Materials
- Process, Tools Yield and Manufacturing
- Advanced Semiconductor Logic Devices
- Memory Technologies
- Photonics, Imaging and Display
- Wide-Bandgap Power, RF Devices and Circuits
- Modeling and Simulation
- Reliability and Testing
- Packaging and Heterogeneous Integration
- Sensor, MEMS, Bio-electronics
- Flexible and Wearable Electronics
- Nanotechnologies
- Neuromorphic & Quantum Technologies
- Bio-Hybrid Electronics (Invited Only)
- On-Chip Thermal Management (Invited Only)
- Quantum Neural Network (Invited Only)

Important Dates

Abstract Submission Deadline
October 1, 2025

Notification of Acceptance
December 12, 2025

Conference Date
March 1-4, 2026

Venue

Setia SPICE Convention Centre - Pulau Pinang, Malaysia

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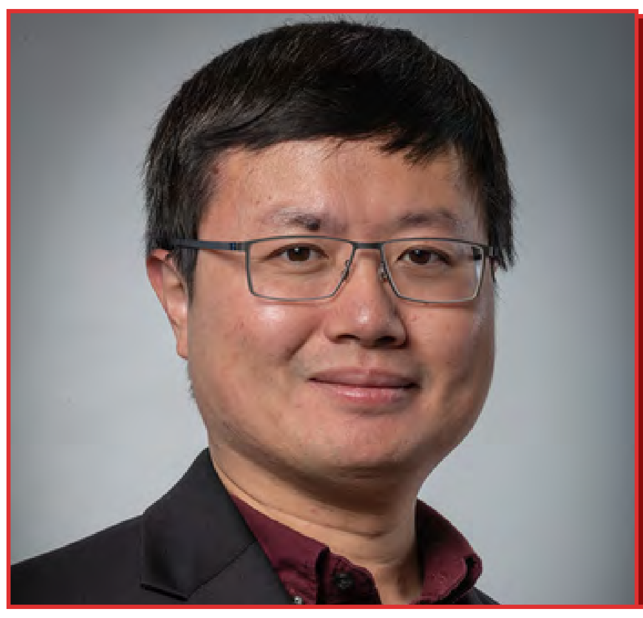
Plenary Speaker

Title : Quantum Computing



Prof. Hiu Yung Wong

San Jose University

Hiu Yung Wong is a Professor at San Jose State University. He received his Ph.D. degree in Electrical Engineering and Computer Science from the University of California, Berkeley in 2006. From 2006 to 2009, he worked as a Technology Integration Engineer at Spansion. From 2009 to 2018, he was a TCAD Senior Staff Application Engineer at Synopsys. He received the Industry Sponsored Research Award and ERFA RSCA Award in 2024, the AMDT Endowed Chair Award, the Curtis W. McGraw Research Award from ASEE Engineering Research Council in 2022, the NSF CAREER award and the Newnan Brothers Award for Faculty Excellence in 2021, and the Synopsys Excellence Award in 2010. He is the author of two books, "Introduction to Quantum Computing: From a Layperson to a Programmer in 30 Steps" and "Quantum Computing Architecture and Hardware for Engineers: Step by Step". He is one of the founding faculty members of the Master of Science in Quantum Technology at San Jose State University. His research interests include the application of machine learning in simulation and manufacturing, cryogenic electronics, quantum computing, and wide bandgap device simulations. His works have produced 2 books, 1 book chapter, more than 130 papers, and 10 patents.

Conference Tracks

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- Memory Technologies
- Photonics, Imaging and Display
- Wide-Bandgap Power, RF Devices and Circuits
- Modeling and Simulation
- Reliability and Testing
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TPC TRACK 1 Materials

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Lance Li

National University of Singapore

Track Co-Chair

Ahmad Sabirin Zoolfakar

Universiti Teknologi MARA, Malaysia

Track Subcommittee

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- Nazek El Atab - KAUST
- Akrajas Ali Umar - Universiti Kebangsaan Malaysia
- Allen Cheah - AT&S
- Yi Wan MSE - National University of Singapore
- Wei yen Won - TSMC, Taiwan
- Hyeon-Jin Shin - GIST, South Korea
- Shi-Jun Liang - Nanjing University, China
- Yan Wang - University of Cambridge, United Kingdom

TRACK 1: Materials

All device-related materials, including **semiconductors, magnetics, ferroelectrics,** insulators and metals, etc. **Smart materials** enabling intelligent devices are highly welcome.

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TPC TRACK 2 Process, Tools, Yield, and Manufacturing

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Tomasz Brozek

PDFSolutions,
USA

Track Co-Chair

Xiao Gong

National University of Singapore (NUS), Singapore

Track Subcommittee

- Anabela Veloso - IMEC, Belgium
- Ratul Baruah - Tezpur University, Tezpur , India
- Heng Wu - Peking University, China
- Yeoh Wai Kong -IME, Singapore
- Dina Tryoso - TEL USA
- Jae-Yong Park- Tata Semiconductors, USA
- Angelo Pinto - Intel, USA
- Tadashi Yamaguchi - Renesas, Japan

TRACK 2: Process, Tools, Yield, and Manufacturing

- Technology development for silicon ICs and other semiconductor devices
- Semiconductor processes and equipment
- Process integration for Logic, Memory, Image Sensors
- Reliability and yield characterization
- Process control and metrology
- Equipment impact on devices
- Self-assembly techniques
- process sensing, FDC (Fault Detection and Classification)
- Analytical and computational tools for Manufacturing and R&D
- AI/ML tools for process development and process enhancement by AI/ML
- Advanced Process Control, R2R, SPC yield analysis and modeling
- Big Data analytics for yield improvement and manufacturing efficiency
- Convergence of Front-End wafer manufacturing and Advanced Packaging

Venue

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TPC TRACK 3 Advanced Semiconductor Devices and Circuits

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Lucy Yang

TSMC, Taiwan

Track Co-Chair

Mohd Khairuddin Md Arshad

Universiti Malaysia Perlis

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- Iskandar Yahya, UKM
- Mousiki Kar, Heritage Institute of Technology, Kolkata, India
- Hsiu-Hau Lin, National Tsing Hua University
- Ming Li, Peking University
- Hock-Chun Chin, NXP
- Lu Ye, Fudan University
- Fong Xuanyao, National University of Singapore
- Mansun Chan, Hong Kong University of Science & Technology
- Yoshiaki Kikuchi, Sony
- Hiroaki Arimura, IMEC, Belgium
- Aimin Song, Southern University of Science & Technology

TRACK 3: Process, Tools, Yield, and Manufacturing

- All semiconductor devices including Si/Ge CMOS,interconnects, compound semiconductors, oxide semiconductors, low-dimensional nanomaterials, ferroelectric, spintronics, 3D devices, Logic for Memory, etc.

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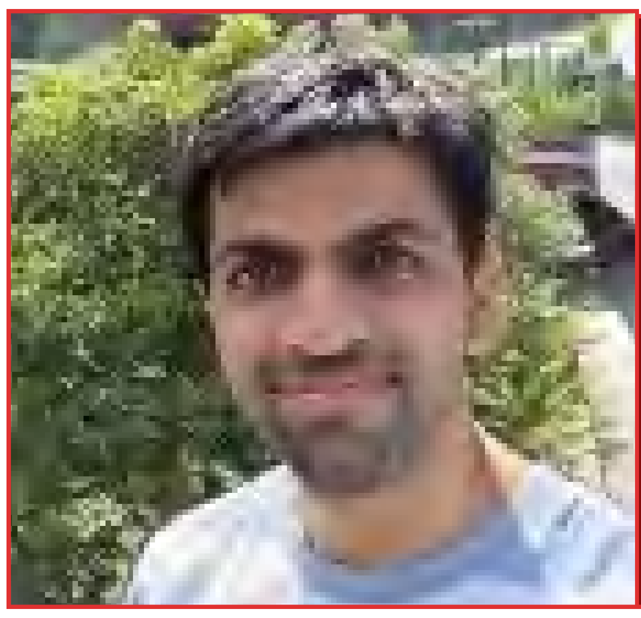
TPC TRACK 4 Memory Technologies

TECHNICAL PROGRAM COMMITTEE

Track Chair



Nagarajan Raghavan

SUTD Singapore

Track Co-Chair

Qianqian Huang

Peking University, China

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- Dee Chang Fu, UKM, Malaysia
- Daphne Chen, Arizona State University, USA
- Sourav De, National Tsing-Hua University, Taiwan
- Damien Deleruyelle, INSA-Lyon, CNRS, France
- Fernando Aguirre, Intrinsic Semiconductors
- Stefan Slesazeck, NaMLab, Germany
- Kechao Tang, Peking University, China
- Jianshi Tang, Tsinghua Univiersity, China
- Andrea Padovani, Univ. of Modena Reggio Emilia, Italy
- Hock-Chun Chin , NXP
- Albert Liao, Micron

TRACK 4: Memory Technologies

- Embedded and standalone, volatile and nonvolatile memories, in-memory and neuromorphic computing, charge-based memories, RRAM, MRAM, PCM, FeRAM, cross-point and selectors, bio-inspired memory, 3D integration, and novel hierarchies/architectures for memory-centric computing.

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TPC TRACK 5 Photonics, Imaging and Display

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Weida Hu

SITP, China

Track Co-Chair

Kausik Majumdar

IISc Bangalore

Track Subcommittee

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- Puvaneswaran Chelvanathan, Universiti Kebangsaan Malaysia
- Kasturi Saha, IIT Bombay, India
- Faisal Rafiq Adikan, Monash University
- Radu Sporea, University of Surrey
- Trupti Ranjan Lenka, NIT Silchar
- Mohd Zamir Pakhuruddin, Universiti Sains Malaysia
- Deep Jariwala, University of Pennsylvania
- Jinshui Miao, Shanghai Institute of Technical Physics, Chinese Academy of Sciences
- Lei Wei, Nanyang Technological University
- Yang Xu, Zhejiang University
- Lei Ye, Huazhong University of Science and Technology

TRACK 5: Photonics, Imaging and Display

- Topics include photonics for energy, optoelectronics, microwave photonics, nano-photonics, optical sensors, optical communications/networking, optical switches, bio- photonics, lasers, optical systems, bio-imaging, imagers, display technology, and other emerging technologies in photonics, imaging, and display.

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TPC TRACK 6 Wide-Bandgap Power and RF Devices/Circuits

TECHNICAL PROGRAM COMMITTEE

Track Chair

Marina Antoniou

University of Warwick

Track Co-Chair

Jagadheswaran A/L Rajendran

Universiti Sains Malaysia

Track Subcommittee

- Victor Veliadis, North Carolina State University
- Sei-Hyung Ryu, Wolfspeed
- Zheyang Zheng, University of Science and Technology of China
- Alberto Castellazzi , Kyoto University of Advanced Science, Kameoka
- Prof. Weifeng Sun, Southeast University
- Ng Wai Tung, University of Toronto
- Man Hoi Wong, Hong Kong University of Science and Technology
- Yuhao Zhang, Hong Kong University
- D Nirmal, Karunya University

TRACK 6: Wide-Bandgap Power and RF Devices/Circuits

- Power device materials such as wide bandgap and ultra- wide bandgap materials (SiC, GaN, AlN, etc.). Discrete and integrated high frequency devices and physics, RF modules and systems, III-V devices for RF application, Active and passive component design for RF.

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TPC TRACK 7 Modelling and Simulation

TECHNICAL PROGRAM COMMITTEE

Track Chair

Manoj Saxena

University of Delhi

Track Co-Chair

Wong Peng Wen

FILPAL

Track Subcommittee

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- Elena Gnani, University of Bologna, Italy
- Anwar Hasan Jarndal, University of Sharjah, UAE
- Technische Hochschule Mittelhessen, Denmark
- Ru Huang, Peking University, China
- Jean Michael Sallese, EPFL, Switzerland
- Hyungcheol Shin, Seoul National University, Korea
- Alex Q Huang, University of Texas, USA

TRACK 7: Modelling and Simulation

- Advances in modeling/simulation of electron devices, packages, and processes. Includes numerical, analytical, and statistical modeling of electronic, optical, or hybrid devices; interconnects; technology CAD; benchmarking; monolithic/heterogeneous integration.

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TPC TRACK 8 Reliability and Testing

TECHNICAL PROGRAM COMMITTEE

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Cher Ming Tan

Chang Gung University, Taiwan

Track Co-Chair

Fei Hui

Zhengzhou University, China

Track Subcommittee

- Marco A. Villena, University of Granada, Spain
- Linfeng Sun, Beijing Institute of Technology, China
- Subhrajit Mukherjee, Shiv Nadar Institution of Eminence, India
- Kaichen Zhu, Fudan University, China
- Abdul Shabir, Center for Reliability Sciences and Technologies, Chang Gung University, Taiwan
- Gan Zhenghao, AMD USA
- Cheong Kuan Yew, Universiti Sains Malaysia
- Udit Narula, Micron USA
- Vimal Pandey, Moxa, Taiwan

TRACK 8: Reliability and Testing

- Reliability of devices, circuits and systems; Design for reliability and variability aware design; Degradation mechanism of emerging devices and memories; stress testing, reliability enhancement techniques, and innovative testing solutions for electronic devices.

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TPC TRACK 9 Packaging and Heterogenous Integration

TECHNICAL PROGRAM COMMITTEE

Track Chair

Goutham Ezhilarasu

UCLA

Track Co-Chair

Atiqah Afzaludin

Universiti Kebangsaan Malaysia

Track Subcommittee

- Gauri Karve, IMEC Belgium
- Eu Poh Leng, NXP
- Genquan Han, Xidian University
- Xin Ou, Shanghai Institute of Microsystem and Information Technology
- Samatha Benedict, Indian Institute of Technology, Dharwad
- Arpan Dasgupta, Global Foundaries
- Haoxiang Ren, Apple
- Yutao Yang, Mediatek

TRACK 9: Packaging and Heterogenous Integration

- 2.1D, 2.5D, and 3D integrations, wafer-level packaging, chiplets, ultra-fine-pitch interconnection, sub-micron package-level wiring, optical/wireless interconnect, power/sensor device packaging, thermal-expansion coefficient, thermal management.

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TPC TRACK 10 Sensor, MEMS, Bio-Electronics

TECHNICAL PROGRAM COMMITTEE

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Yao Zhu

A-Star, Singapore

Track Co-Chair

Jumril Yunas

Universiti Kebangsaan Malaysia

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- Zhiqin Chu, University of Hong Kong
- SMing He, Peking University
- Badariah Bais, UKM, Malaysia
- Arjun Kantimahati, Silterra
- Mohd Nizar Hamidon, UPM Malaysia
- Azrul Azlan Hamzah, UKM, Malaysia
- Rhonira Latif, UKM Malaysia
- Roer Eka Pawianto, UPI Indonesia
- Kyeongha Kwon, KAIST
- Taeko Ando, Ritsumeikan University
- Wang Nan, Shanghai University

TRACK 10 : Sensor, MEMS, Bio-Electronics

- Advances in sensors, transducers, and actuators; Intelligent sensors with embedded AI; MEMS/NEMS devices; Microfluidics and BioMEMS; CMOS on MEMS; RF MEMS; Micro-optical and opto-chemical devices; MEMS for energy harvesting and on-chip energy storage; Bio-sensors

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TPC TRACK 11 Flexible and Wearable Electronics

TECHNICAL PROGRAM COMMITTEE

Track Chair

Shweta Agarwala

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Track Co-Chair

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Universiti Malaya

Track Subcommittee

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- Sharifah Fatmadiana Bt Wan Muhammad Hatta, Universiti Malaya
- Syed Muhammad Hafiz, MIMOS Bhd
- Chen Jiang, Tsinghua University
- Anis Nurashikin Nordin, International Islamic University Malaysia
- Madhu Bhaskaran, RMIT, Australia
- Feng Yan, The Hong Kong Polytechnic University Hung Hom, Kowloon, Hong Kong
- Dipti Gupta, IIT Bombay, India
- Aditya Sadhanala, IISc, India
- Panote Thavarungkul, Center of Excellence for Trace Analysis and Biosensor, Thailand
- Yang Joel, SUTD, Singapore

TRACK 11 : Flexible and Wearable Electronics

- Flexible devices for wearable applications; Materials for flexible electronics.

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December 12, 2025

Conference Date
March 1-4, 2026

Venue

Setia SPICE Convention Centre - Pulau Pinang, Malaysia

Short Course

EDTM 2026 will start with a set of short courses and tutorials on March 01, 2026. Tutorials will cover selected topics from the basics to the state-of-the-art.

Publication Opportunity

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Abstract Submission Deadline
October 1, 2025

Notification of Acceptance
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TPC TRACK 13 Neuromorphic, Quantum and Disruptive Technologies

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TRACK 13: Neuromorphic, Quantum and Disruptive Technologies

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Abstract Submission Deadline
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